Hot-carrier Reliability Characterization of Advanced CMOS Devices

The semiconductor industry is currently driven by continuous device scaling in order to keep up with Moore's law. Unfortunately, this has resulted in increased electric fields and operating temperature with more and more devices placed on a single chip. As a result, various reliability challenges pose a threat to the performance of integrated circuits. One such reliability concern is the hot-carrier degradation (HCD) that affects transistor parameters and consequently, functionality of various analog and digital circuits severely. The time-evolution of HCD in MOSFETs has traditionally been studied to predict device performance during its lifetime. HCD curve follows a power-law with the time-exponent of degradation being an important measure. This variation in time power-law exponent for different stress bias combinations or over different stress time intervals can be used to identify the major degrading mechanism during HCD.

HCD studies involving accelerated testing render inaccuracy when employed on advanced MOS devices such as silicon-on-insulator (SOI)-FETs. The use of continuous DC supply as stress voltage results in device-heating or self-heating (SH). This local temperature build-up within the device is known to enhance hot-carrier injection (HCI) in the gate dielectric of the device. Also, the use of a fixed DC stress voltage is overly pessimistic as it is seldom encountered in a real circuit operation. In general, the effective duty cycle of the voltages or currents applied to a device during a circuit operation will always be less than 100%. This demands for a revision in conventional stress set-up with the use of DC stress input being replaced by pulsed or AC stress waveforms.

Stress-induced performance drifts have become common in RF circuits as well. Often during the circuit operation, the constituent transistors are exposed to high voltage, high current regimes thereby, making them vulnerable to HCD. Therefore, device technology qualification in terms of its DC as well as RF performance parameters is required. Moreover, understanding the device performance under RF operating conditions has also become critical. Therefore, formulating the methodologies and techniques such that the device is stressed under realistic random logic circuit operating conditions with input bias chosen as per the target DC or RF application is necessary.