ABSTRACT

Performance degradation due to early device-aging has been a critical concern for semiconductor industry. High electric fields within the device channel lead to several reliability concerns hindering further downscaling at advanced technology nodes. Hot-carrier degradation (HCD) is one such dominant aging mechanism in present-day integrated circuits. For a device under hot-carrier stress (HCS), threshold voltage (V_{TH}) gradually increases over time which can affect the speed of the encompassing circuit leading to operation failure. Several factors including external operating conditions like temperature, nature of applied stress bias (asynchronous/synchronous pulse, DC, RF), and frequency of operation etc. affect the performance of a circuit due to HCD. In addition, V_{TH} variations may occur in a device due to increased process variability at nanoscale dimensions as well. Therefore, a thorough understanding of these issues is needed to ensure required device lifetime and accurate functionality.

This work addresses HCD aging from two major perspectives; first, accurate age monitoring and identification of dominant degrading mechanisms. In order to implement guard-bands for failure-prevention, critical biases affecting device performance at different technology nodes are determined. However, issues peculiar to device geometries, such as increase in series resistance in narrow fins, increased local device-temperature due to dense layouts, change in V_{TH} at narrow dimensions etc. may change the effective stress bias reaching the channel. Thus, the geometrical implications of HCD are studied to determine most degrading bias combinations. The second perspective deals with the effect of device scaling on HCD. Conservative performance metrices, such as ON-current, V_{TH} or subthreshold slope are studied along with OFF-state leakage current and drain-induced barrier lowering, for holistic analysis of device performance in different operation regimes. Moreover, dynamic workload i.e. pulsed asynchronous stress is used for optimizing guard-band, which is otherwise too strict if based on DC stress conditions. Also, RF metrices are investigated using S-parameters showing that the mechanisms affecting DC and RF device performance are necessarily the same.