

Abstract of Ph.D. Thesis
“Design, Control and Development of Single Phase Multilevel Converters for PV Based Grid-Tied Applications”

Ms. Nidhi Mishra (2013EEZ8528)

Multilevel converters (MLCs) are capable of providing power transfer at lower harmonics distortion, reduced switching stresses, less electromagnetic interference, and minimum filter size. The multilevel inverters increase the voltage to a level above than rating of semiconductor switches by connecting them in suitable arrangement. A high voltage stepped wave closer to a pure sine wave is main motive of bringing such multilevel converters. Various topologies like neutral point clamped (NPC) converter, cascaded H bridge (CHB) converter and flying capacitor (FC) are available in the literature. Higher number of levels provide above-mentioned advantages but at the cost of an increase in converter structure. The system must be compact and cost-effective to be accepted in the practical system. Various low switching frequency based medium voltage multilevel converters are implemented to adhere with minimum switching losses and keeping harmonic standards in an acceptable limit. A major disadvantage of conventional topologies, is that switches are increased drastically increasing controller complexity, switching losses, and financial burden. Hence, moving towards reduced number of semiconductor switches, DC-link capacitors, flying capacitors, and clamped diodes to cater such issues, various topologies have come up in the field of multilevel converters. The CHB configurations with symmetric and asymmetric sources are investigated for five and seven-level grid-connected PV array fed applications. A prototype of five-level CHB is implemented and its performance is analyzed at variable irradiances and abnormal conditions using solar PV emulators. Moreover, NPC and active NPC topologies with neutral point voltage balancing and flying capacitor control have been incorporated in this work. Furthermore, packed U-cell (PUC) topologies for seven, eleven and fifteen level output voltage, are presented for closed loop solar photovoltaic grid-tied applications. The modified PUC with voltage boost mode capability is investigated in closed-loop system and input DC sources need not be higher than PCC voltage. An eight switch eleven level reduced switch count topology is one of the main contribution of the thesis. A new topology with twenty-five level output voltage generation with twelve active switches is incorporated in the work for solar photovoltaic grid-tied applications. Moreover, a nearest level modulation strategy is incorporated to achieve fundamental switching and minimum switching losses. The multiple topologies are covered in closed-loop single-phase single stage grid-connected configurations. The incremental conductance (INC) and perturb and observe maximum power point techniques are implemented within the inverter control to have single-stage configuration. The efficiency of single-stage makes it more viable as compared to extra boost conversion stage in double stage configurations. The power quality indices are worked and results are found compliant with the IEEE 519 and IEEE 61727 standards. Moreover, real-time testing of such topologies is executed using rapid prototyping based digital simulators. Few topologies are run in RT-LAB environment at physical clock time in hardware synchronization mode. Moreover, some topologies are simulated using MATLAB/Simulink and results are validated using hardware laboratory setup and in hardware in loop (HIL) using OPALRT real-time digital simulator (RTDS). These systems are evaluated in terms of cost-effectiveness, reduced switch count, power quality standards, simplicity, robust control, and practical feasibility.