SAR A/D-Converter Techniques for Array Applications

A THESIS

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by

Sanjoy Kumar Dey

under the guidance of

Prof. Mukul Sarkar

Prof. Shouribrata Chatterjee

Indian Institute of Technology Delhi

Department of Electrical Engineering

INDIAN INSTITUTE OF TECHNOLOGY DELHI

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ABSTRACT

Analog-to-digital converters (ADCs) for array applications, e.g., CMOS image sensors, requires optimization in both area to reduce cost and power to reduce energy consumption for increased battery life. For high dynamic range (HDR) imaging, the required resolution and noise performance also increases. Successive approximation register (SAR) ADCs are very popular for their proven energy efficiency, but typically area inefficient compared to other architectures.

The research work in this thesis is centered around low-area and low-power SAR ADC for array applications. Three major improvements were incorporated in the circuit design to achieve the goal. Finally, a test chip was fabricated and meausred to validate the proposed improvements. Test-chip silicon measurement results are presented.

A capacitor distribution mechanism is introduced with mathematical analysis followed by simulation results to improve noise, without increasing the power consumption, of the strong-arm latch-based dynamic comparator. This technique shows that the distribution of the additional noise control capacitor in a specific ratio between integration and regeneration nodes yields the best energy efficiency.

To reduce the power consumption of the comparator without impacting input-referred noise, a self-shut mechanism was introduced with detailed mathematical analysis and simulation results. The silicon measurement conformed to the proposed technique. The average saving of current consumption for stand-alone comparator working for SAR ADC binary search ranges from 20%-40%, and overall ADC power improvement is ~8-10%. As this does not impact the noise performance, the improvement is trade-off free.

To reduce area, an all-digital mismatch-calibration technique with a novel mechanism of reuse of capacitors for mismatch error measurement, error correction, sampling, and conversion was introduced with detailed methodology and analysis. The MATLAB simulation results were presented to verify the proposal. Reusing the capacitors ensures that extra capacitors for calibration are avoided, hence saving area. As the calibration is on-chip, costly factory testing and trimming (NVM memory or fuse bits) are also avoided. This overall improves the area and cost of the SAR ADC.

A prototype ADC is carried out in a 65-nm technology to test all the proposals. With these three techniques together, an INL of 2.9 LSB at 14-bit and ENOB better than 11.3-bit is achieved by the ADC while operating at 6.7 MS/s. The achieved energy efficiency FoM_W is 5.8 fj/conv-step, and FoM_S is 175 dB with an area efficiency of 5.9 μm^2/code. The proposed changes are scalable for higher-resolution ADCs. The autocalibration is digitally heavy to take care of all process and tool imperfections in the digital domain. This ensures a first silicon success without requiring any mask re-spin, making it highly portable across technologies for good yield in high-volume manufacturing. When shared across 10 columns with a 5.6 μm pitch, this area-efficient auto-calibrating ADC can deliver 670 frames/s video for a 1-megapixel array.