Abstract of PhD Thesis
Topic: "Modeling and Control of Low-Voltage Common DC Bus-Based Multi-Converter Architecture"
Name: Mr. Himansu Sahoo (2019EEZ8506)

ABSTRACT

The objective of this research is to analyse various modeling and control approaches for a common direct current (DC) bus-based interconnected converter configuration. Considering the basic control logic for power converters connected to a common DC bus, two-loop control, with the inner loop as average current control, is most commonly used. However, the presence of two controllers per converter makes the modeling and controller tuning processes analytically complex for a multi-converter system. To simplify the tuning process and reduce model complexity, in the initial stage of the work, the reduced-order modelling approach with mixed-signal peak-current control logic is analysed for distinct DC-DC converters as well as for the overall interconnected system. Presented coupling effects among converters in the interconnected structure are considered in the modeling process. The effect of a constant-power-type load with exact and approximate model behaviour is also thoroughly investigated. Developed analytical models are verified against a circuit-based simulation model to assess accuracy. A detailed analysis of controller design and stability assessment is carried out. The states of the power converters are formulated in a generic form to be easily expressed for additional future units.

In a further stage of analysis, emphasising the practical use of such an interconnected architecture, a standalone DC common-bus-based structure is considered. Such architecture adheres to multi-mode functionality and multiple control laws. Each mode is analysed and modelled properly to develop the required control parameters. The control logic is implemented in inner-peak-current mode, with additional ramp compensation to ensure stable system operation across a wide operating range of power converters. To ensure smooth mode reversal as per load and source requirements, a simplified, reduced-sensing-circuitry logic is developed based on DC bus information. The common bus voltage is predicted from the sensed output voltage and the current of any of the source-side converters, and the mode-shifting logic is implemented using this predicted information. It helps avoid the complexity of direct bus voltage sensing. To enhance the operational flexibility of the low-voltage DC bus, the architecture requires a connection to the community DC bus, which is realised via high-gain converters. For this purpose, a cascaded boost converter design is analysed across different operating intervals and various switching-frequency settings of the primary and secondary power stages.

Interactions among power topologies within the multi-converter structure affect the dynamic response of the common bus. Moreover, the coupling effect is directly observed in the system modelling process. To improve dynamic response, feed-forward-based control logic is added, with a peak-current-based control loop, and a trajectory-based tuning approach is used to make the controller parameter design process independent of the power topology. For the direct implementation of the developed control parameter in the digital controller platform, a discrete-time modeling approach is analysed for a parallel-connected structure. An investigation into the stability boundary for changes in various system parameters is conducted. The control parameters derived from the developed models are validated on a hardware prototype to demonstrate the required regulated system functionality.