Thesis title:

Power management circuits for energy-harvesting systems

Abstract:

The thesis showcases power management circuits for energy-harvesting systems. The contributions of the thesis are as follows:

AC-DC power conversion techniques for energy harvesting from piezoelectric transducer: Phase-locked loop (PLL)-based rectifier-less power switching converter, multi-step charge transfer interface circuit, and CMOS-only undervoltage lockout circuit with dual mode operation.

Ultra-low-power reference circuits: Dual loop self-regulated CMOS-only voltage reference and a single BJT-based voltage and current references.

Nanoampere-level quiescent current low dropout regulators: A gm-boosted flipped-voltage-follower (FVF) based output-capacitor-less LDO with fast transient response and a multi-feedback-loop LDO.

A sub-1V LDO with built-in single BJT-based bandgap reference.

A PLL-based rectifier-less interface circuit is proposed to control the power switches for harvesting energy from a low-voltage piezoelectric transducer, with input power levels ranging from 100 nW to 40 μW. In this method, the charge-pump PLL is first locked to the piezoelectric energy harvester (PEH) input frequency to detect the PEH's peak output voltage, thereby maximizing power extraction. Once locked, power transfer occurs with the PLL operated in open loop (only the voltage-controlled oscillator (VCO) is functional) to minimize power loss. In 180 nm CMOS technology, the power switching converter was designed to extract power with a minimum piezoelectric open-circuit voltage of 0.17 V. At an input power of 10 μW and a vibration frequency of 88 Hz, it achieves a maximum power efficiency of 84%. To extract the maximum available input power from a piezoelectric energy harvester, a highly power-efficient interface circuit based on a multi-step charge transfer (MSCT) technique is proposed. The MSCT approach pre-charges the piezoelectric capacitance, flips the piezoelectric output voltage, and extracts the stored charge in multiple stages. This technique enhances the end-to-end power efficiency of the rectifier by reducing conduction losses in the power converter stage while extracting the maximum possible stored energy from the piezoelectric intrinsic capacitance for a given CMOS process. The proposed rectifier is designed and simulated in a 0.18-μm CMOS process. Under the same input power conditions, the rectifier extracts 14.39 μW and 16.34 μW of output power with one-step and four-step charge transfer, respectively. The MSCT achieves maximum power efficiencies of 68.5% with a 47 μH inductor and 83% with a 220 μH inductor. Simulation results demonstrate that the MSCT

technique with four steps yields a 13.85% enhancement in power efficiency relative to single-step charge transfer. For reliable operation of the interface circuit, a charge-monitor circuit, also known as under-voltage lockout, is required. An ultra-low-power, CMOS-only undervoltage lock-out (UVLO) circuit is proposed for energy-harvesting applications. The proposed UVLO operates in a dual-mode configuration, which is essential for energy-autonomous power-switching convert-ers, while consuming significantly less area and power than conventional bandgap-based UVLOs that require multiple resistors and BJTs. The design is fabricated in a 0.18 μm CMOS technology and occupies an active area of 0.0066 mm^2. The measured low-to-high trip voltage ($LHTV_1$) and high-to-low trip voltage ($HLTV_1$) for the first mode are 1.362 V and 1.018 V, respectively, while the $LHTV_2$ and $HLTV_2$ for the second mode are 1.608 V and 1.492 V, respectively. The circuit consumes a quiescent current (I_Q) of 300 pA at room temperature under a 1.8 V supply.

To achieve ultra-low-power operation and occupy a small area, energy-efficient and area-efficient reference circuits are proposed. A picowatt CMOS-only voltage reference (VR) that improves the line sensitivity (LS) using a dual self-regulation circuit while consuming a small area and power. The proposed design has been implemented in a 65 nm CMOS low power (LP) process and occu-pies an active area of 1373 μm^2. The post-layout Monte Carlo simulation shows that the circuit gives an average reference voltage of 287 mV and a standard deviation of 10.32 mV. The line sen-sitivity is 0.59%/V across the supply voltage range from 0.5 V to 1.2 V, and it drops to 0.036%/V when the power supply sweeps from 0.8 V to 1.2 V. The circuit consumes 70 pA of quiescent current from a 0.5 V supply at room temperature. To generate a reference voltage and current that are insensitive to process variations, a single bipolar junction transistor (BJT)-based voltage-current reference (VCR) is proposed, combining both in a single circuit. In the proposed design, a β-multiplier produces a proportional-to-absolute-temperature (PTAT) voltage, which is summed with a fractional BJT emitter-base voltage (V_{EB}) having complementary-to-absolute-temperature characteristics, to obtain a temperature-compensated reference voltage (V_{REF}). The reference current (I_{REF}) is obtained from the ratio of V_{REF} to a temperature-compensated resistor (TCR), implemented as a series connection of a CTAT unsilicided P+ poly resistor and a PTAT N-well resistor. The proposed circuit is implemented in a 65-nm CMOS technology and occupies an area of 0.1 mm^2. Results from post-layout Monte Carlo simulations demonstrate that V_{REF} and I_{REF} achieve average temperature coefficients of 13.9 ppm/°C and 83.85 ppm/°C, respectively, over the temperature range of −40 °C to 120 °C. The average V_{REF} and I_{REF} values are 243.34 mV and 9.97 nA, with standard deviations of 2.49 mV and 454 pA, respectively. The circuit operates from a 0.85 V supply and consumes 113 nW power at 120 °C.

Furthermore, the power management unit (PMU) is designed for energy-efficient applications that demand an ultra-low I_Q low dropout regulator (LDO) to provide a clean and regulated supply for a wide range of load currents. In this thesis, an ultra-low quiescent output-capacitor-less low-dropout regulator (OCL-LDO) with enhanced load regulation is proposed. The LDO architecture is based on a FVF topology, where the Gm stage with a current-mirror load replaces the constant-current source of the folded-cascode common-gate amplifier to improve DC load regulation and transient performance. A super-source follower (SSF), which acts as a voltage buffer, is inserted

to drive the high-power transistor. Furthermore, a dynamic sensing unit is utilized to achieve a fast settling time during a low-to-high load step. In a 65 nm low-power CMOS process, the proposed LDO was designed. The LDO consumes 95 nA of quiescent current and can deliver up to 50 mA of load current with a 1.2 V supply and a 1 V regulated output. It achieves a DC load regulation of 14.8 mV/A by varying the load current from 500 nA to 50 mA. With a 100 pF load capacitor, the output voltage undershoot is 626 mV with a 100 ns rise time and reduces to 530 mV with a 200 ns rise time for a full-load-step current, settling within 350 ns. To achieve the best trade-off among quiescent current, area, and other LDO parameters, especially line/load regulation, settling time, and maximum load current, an ultra-low-power, output-capacitor-less low-dropout regulator (OCL-LDO) with a multiple-feedback loop (MFL) is proposed. The proposed LDO comprises five feedback loops that deliver excellent steady-state and transient performance. A tri-loop FVF stage enhances both line and load regulation. The slew-rate enhancement loop based on a source cross-coupled error amplifier (SXCEA) provides a fast transient response. Moreover, the proposed LDO utilizes a dynamic feedback loop that significantly improves undershoot recovery time during the full-load step current. The proposed LDO was fabricated in a 65-nm CMOS node with an active area of 0.025 mm^2. The LDO can deliver a maximum of 50 mA load current at a 1 V output voltage and consume only 22 nA measured quiescent current. The measurement results show that the proposed LDO achieves a load regulation of 0.004 mV/mA and a low-frequency power supply rejection (PSR) at full load of −63.5 dB. For a load current step from 200 nA to 50 mA with a 10 ns edge time, the measured voltage undershoot is 574 mV and settles within 200 ns.

To further reduce overall area and power consumption, a fully integrated, low-power, low-voltage, low-dropout regulator is proposed that shares the feedback resistors of the LDO with a single BJT-based voltage reference. The proposed architecture uses only one BJT and two resistors to generate a temperature-compensated, regulated output voltage, unlike conventional reference-integrated voltage regulators, which require multiple BJTs and resistors. Additionally, by reducing the V_{EB} of the BJT to half its value using a voltage divider circuit, the design achieves sub-1V operation. Hence, the proposed LDO offers both area and power efficiency. The proposed architecture was fabricated in a 65-nm low-power CMOS node and occupies a die area of 0.017 mm^2. The LDO delivers a maximum load current of 10 mA at a nominal output voltage of 0.608 V. Measurement results show that the LDO achieves a temperature coefficient (TC) of 26.2 ppm/°C from −40 °C to 120 °C, and a voltage precision of 0.499 %. The measured line regulation and load regulation are 3.925 mV/V and 0.12 mV/mA, respectively. The LDO consumes 241 nW of power with a minimum supply voltage of 0.8 V.