Abstract

As information density reaches the petascale level (10^{15}), power density also increases, presenting a significant challenge in achieving higher bit densities while maintaining power-efficient systems. The human brain is an exemplary model of an energy-efficient system, utilizing ternary synaptic weights to process information while consuming only about 20 W, despite having petascale connection densities. Motivated by this efficiency, neuromorphic architectures and brain-inspired designs have been developed, which offer a promising solution to overcome the power scaling limitations of traditional Von Neumann computing, making it a viable alternative for energy-efficient, large-scale processing.

The energy and area efficiency of neuromorphic architectures can be further enhanced by scaling down MOSFETs, reducing power supply voltage, and implementing multivalued logic. MOSFETs serve as the fundamental building blocks of neuromorphic computing. Scaling down MOSFETs increases area efficiency but simultaneously exacerbates short-channel effects (SCE), which in turn leads to higher power dissipation. Although power dissipation can be reduced by lowering the supply voltage, this cannot be done indefinitely due to the limitation of the subthreshold swing, which cannot scale below 60 mV/decade. This phenomenon, referred to as the 'Boltzmann tyranny,' arises from the thermionic injection current mechanism inherent in conventional MOSFETs.

Tunnel field effect transistors (TFETs) offer a promising solution by employing band-to-band tunneling as the current conduction mechanism, enabling subthreshold swing below the 60 mV/decade limit. However, several challenges must be addressed to fully harness the potential of TFETs compared to conventional MOSFETs. A key limitation of TFETs is the relatively low drive current resulting from the band-to-band tunneling (BTBT) mechanism in the ON state.

Another alternate way to increase power and area efficiency is to use multivalued logic, such as ternary logic. Ternary logic stores more than two logic levels, in contrast to binary logic, reducing the number of devices needed resulting in decreased power dissipation. Based on three logic states, ternary logic reduces system complexity by 63% compared to binary logic. Conventional CMOS ternary systems use a multiple threshold voltage scheme, which results in high power dissipation due to constant current flow. Alternatives like enhancement/depletion-

mode MOSFETs and innovative devices such as carbon nanotube FETs, negative capacitance FETs, and tunneling based ternary CMOS (T-CMOS) offer lower power solutions. T-CMOS offers the lowest static power dissipation because it uses band-to-band tunneling to generate the third voltage state. However, the other two logic states are generated due to conventional thermionic emission, which prohibits the supply from scaling down.

Therefore, in this thesis, we have designed a novel nanotube tunnel FET (NT-TFET) to enhance the ON-state current and achieve steep switching in emerging nanotube tunnel FETs, aiming for next-generation low-power, high-speed devices in sub-10 nm technology nodes. Furthermore, this device is optimized for implementing a standard ternary inverter operating at a 0.5 V supply for low-frequency and low-power, area-efficient neuromorphic systems. Finally, its potential is explored in the implementation of balanced ternary logic.

Firstly, a novel design featuring a gate-overlapped-source-only nanotube tunnel FET (GoS-NT-TFET) configuration was proposed, which aligns the tunneling path in the direction of the gate electric field, a mechanism known as line tunneling. This proposed device demonstrates a steep average subthreshold swing (SS_{avg}) of 30 mV/decade and an ON current approximately 24 times higher than that of the conventional NT-TFET, even at a low supply voltage of 0.5 V.

Secondly, the GoS-NT-TFET is optimized for ternary operation, demonstrating gate-bias-independent point tunneling at low gate bias and gate-bias-dependent line tunneling at higher gate bias. This device was meticulously optimized by varying the channel length, source doping, and drain doping. The standard ternary inverter (STI) designed with the optimized device shows an impressive three-order reduction in static power dissipation, ~50% improvement in dynamic power dissipation, and ~49% improvement in the power delay product (PDP) compared to the conventional T-CMOS.

To further enhance the performance of the STI, we propose a drain side pocket-based Germanium nanotube tunnel field-effect transistor (DP-LNTFET). This innovative device showcases a ~ three orders of magnitude increase in ON-state current, and ~ three orders decrease in the delay compared to the GoS-NT-TFET, making it suitable for operation in the kHz frequency range. Moreover, the STI implemented with DP-LNTFET demonstrates a significant ~156% improvement in static noise margin (SNM) and ~97% improvement in the PDP, compared to the STI implemented with the conventional T-CMOS device. The potential impact of process variations on the performance of the STI is also analyzed,

where the DP-LNTFET shows invariance to doping profile variations at the pocket and drain junction, thereby reducing doping complexity.

The DP-LNTFET is further explored for implementing various balanced ternary logic circuits. A novel methodology is proposed for designing ternary logic using single-threshold DP-LNTFETs, eliminating the need for conventional multi-threshold devices and passive components. Pre-charging techniques to reduce delay without degrading the power delay product (PDP) are investigated, with the most effective approaches applied to implement key ternary logic gates such as the Negative Ternary Inverter (NTI), Positive Ternary Inverter (PTI), Not Accept Anything (NANY), and Non-Consensus (NCONS) gates. A balanced ternary full adder (BTFA) is also designed, showcasing a ~48% improvement in PDP at a low supply voltage (V_{DD} = 0.5 V) compared to its T-CMOS counterpart.