BROADBAND TRANSMIT/RECEIVE FRONT END FUNCTIONAL BLOCKS USING GAN TECHNOLOGY

by

Ashish Jindal

CENTRE FOR APPLIED RESEARCH IN ELECTRONICS, IIT Delhi

ABSTRACT

This thesis presents the design, development, and full monolithic integration of a
This thesis presents the design, development, and full monolithic integration of a
broadband, high-power, and compact Transmit/Receive (T/R) front-end module using Gallium Nitride (GaN) Monolithic Microwave Integrated Circuit (MMIC) technology. It is motivated by the growing demands of modern radar and electronic warfare (EW) platforms, which increasingly rely on wideband, high-efficiency, and space-constrained phased array architectures. This research addresses key challenges associated not only with the development of individual functional blocks but also with the integration of high-performance Low Noise Amplifiers (LNAs), Power Amplifiers (PAs), and RF single pole double throw (SPDT) switches onto a single MMIC chip.

The dissertation presents novel design methodologies and circuit-level innovations across three critical RF building blocks: LNAs, PAs, and Single Pole Double Throw (SPDT) switches. A key innovation is the introduction of a Rotation-Aligned Interstage Matching (RAIM) technique for wideband LNAs. This approach counters the impedance trajectory mismatch caused by Foster’s reactance theorem and the inherent characteristics of HEMTs, enabling optimal conjugate matching between amplifier stages without

intermediate 50-ohm terminations. As a result, substantial improvements in noise figure, gain flatness, and return loss are achieved across multi-octave frequency spans.

In the domain of power amplification, an improved Non-Uniform Distributed Power Amplifier (NDPA) topology is proposed and implemented. The design introduces a novel method for determining the characteristic impedance of the drain transmission line, ensuring it remains within a realizable range and can be directly matched to 50 ohms. This approach eliminates the need for bulky output transformers, significantly reducing chip area and insertion loss. To maintain consistent efficiency across all stages, the input drive levels are strategically adjusted, allowing each stage to operate optimally under its specific load conditions. The resulting amplifier achieves output power levels exceeding 10 W with high power-added efficiency, typically around 30%, across the 4–19 GHz frequency range.

For the switching function, a compact and broadband SPDT switch is developed based on an Active Loaded Transmission Line (ALTL) structure, combined with inductive tuning to achieve the desired frequency band and support high power handling. The resulting design demonstrates exceptional performance, with isolation exceeding 50 dB, insertion loss below 0.8 dB, and power handling capabilities above 43 dBm across the 4–20 GHz band. Furthermore, the switch is integrated with an on-chip driver that generates appropriate gate control voltages, thereby eliminating the need for external high-voltage control circuitry. To further enhance power handling, cascading of series devices is employed, enabling the switch to achieve a power handling capability of up to 44.5 dBm with insertion loss below 1 dB over the 1–18 GHz range.

These building blocks are monolithically integrated into a Single-Chip Front-End (SCFE) MMIC, combining the LNA, PA, and SPDT switch into a unified compact architecture. The SCFE achieves broadband operation from 4.5 to 18 GHz, with transmit output power exceeding 9 W, receive-mode noise figure below 3.5 dB, and Tx-Rx isolation surpassing 55 dB. Multiple SCFE prototypes are fabricated and evaluated to address coupling, layout optimization, and electromagnetic isolation challenges, progressively improving overall performance metrics.

The outcomes of this research represent a significant advancement in GaN-based MMIC design, offering practical solutions to the long-standing challenges of wideband impedance matching, high-power integration, and on-chip control compatibility. The presented architectures lay the foundation for the next generation of multifunctional, reconfigurable, and SWaP-optimized RF front ends, with direct applicability in phased-array radars, EW receivers, and high-speed communication platforms. This work contributes not only to the state-of-the-art in MMIC integration but also provides a scalable framework for future developments in frequency-agile and digitally controlled RF systems.