Real time compressive sensing in CMOS image sensors

Abstract

CMOS image sensors are widely used in imaging applications ranging from simple photography to scientific measurements. The parallelism followed in image sensors generates an enormous amount of data that makes storage/processing a challenging task. Image compression techniques ease this task by reducing the amount of data while increasing the power consumption of the processing blocks. However, image compression reduces the power consumption involved in signal transmission. Thus, image compression introduces a trade-off between the power consumption of the processing and communication blocks of the imager. Hence, image compression schemes that lead to an overall reduction in power consumption are highly desirable.

The number of pixel outputs sensed and processed by the compressive sensing imagers is smaller than the number of pixels corresponding to the imager's spatial resolution. However, the image quality depends on the reconstruction algorithms, which demands extensive training. Feature-based and information-centric bio-inspired compression algorithms exhibit higher energy efficiency than the information-theory based compressive sensing algorithms. Besides, most of the works reported in the literature focus on reducing the spatial or temporal resolutions to reduce the power consumption. Compression on the depth of the pixel is rarely used.

In this work, the photon shot noise characteristic of an image sensor is used to achieve bit-depth compression. The photon shot noise-inspired image sensors use increased quantization step sizes at high light conditions to accelerate the data conversion in slope ADCs. Here, an accelerated ramp with uniform counting is proposed to achieve bit-depth compression. The power consumption of the image sensor readout with slope ADCs can be reduced using low-power bandwidth-limited preamplifiers as the first stage of the comparators. The limited bandwidth introduces latency in the data converter output. In this work, a comparator with a switching accelerator is designed in a 0.18 μm CMOS process to reduce the latency without increasing the static power consumption of the comparator. The switching accelerator also increases the switching speed of the comparator.

Slope ADCs using accelerated ramps result in slope-dependent nonlinearities

in their transfer characteristics. A decelerated-ramp slope ADC ensures unique digital outputs for each analog quantization range, thus reducing nonlinearity. A decelerated-ramp slope ADC designed in a 0.18 μm CMOS process has no missing decision levels even with bandwidth-limited comparators. The nonlinearities due to slope-dependent latencies are reduced to less than 0.5 LSB. With reduced nonlinearity, a second-level compression can be applied to the bit-depth compressed outputs.

A two-level image compression using our bit-depth compression followed by Discrete Cosine Transform is proposed. The two-level compression achieves a PSNR of 48.9 dB and an SSIM of 0.99 for a quality factor Q=16. The resultant PSNR and SSIM are 5.5 dB and 0.0126 higher than the transform domain compression without bit-depth compression for the same quality factor and equal data rate.

The bit-depth compression supports a higher resolution ADC with fewer bits for its digital representation. The advantages of the proposed bit-depth compression in a depth-sensing application are studied using the measurement results of a time-of-flight sensor fabricated in a 0.35 μm AMS OPTO process. The increased ADC resolution predicts a reduced error in the distance measurement compared to a linear readout. The approach has been realized in an imager designed in a 0.35 μm OPTO process. The available characterization results show that the circuit design techniques need further improvement to demonstrate our proposed approach.

In summary, the proposed PTC-inspired bit-depth compression can reduce the power consumption of imager readouts. As the bit-depth compression is near-lossless, a second-level compression is also possible. Our bit-depth compression can realize high-resolution ADCs with less number of bits. The increased ADC resolution can provide more accurate measurements in sensing applications.