CARRIER-SELECTIVE CONTACTS BASED SILICON HETEROJUNCTION SOLAR CELLS: FABRICATION AND DEVICE CHARACTERIZATION

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ABSTRACT

For the general use of solar photovoltaic devices, the device fabricated with commercially viable silicon wafers at room temperature is preferable to harvest abundant solar energy. With this motivation, we have fabricated carrier-selective contact (CSC) based silicon heterojunction solar cells at room temperature, based on carrier-selective layers without using any specified surface passivation layer on a silicon wafer. Industrially feasible Cz n-type non-textured silicon wafers having the bulk lifetime of 300 μs have been used for the device fabrication. The molybdenum oxide (MoO_x) and lithium fluoride (LiF_x) have been used as the hole- and electron-selective layers, respectively. We have achieved the highest conversion efficiency of >15% from the simple architecture of Ag/TCO/MoO_x/n-Si/LiF_x/Al completely processed at room temperature. The internal quantum efficiency of ~96% has been observed in the shorter wavelength region, whereas to understand relatively less response between 800 to 1100 nm wavelength region; effective minority carrier diffusion lengths have been estimated. We also confirmed the inversion layer formation in the silicon after MoO_x contact from temperature-dependent capacitance-voltage measurements and quantified the crucial built-in-potential of ~0.69 V from the cell structure due to the high work function of MoO_x layer, which has led to the open-circuit voltage of the device to ~0.57 V.

Further, the device characteristics have also been investigated by dark/light current density-voltage characteristics, and the MoO_x/n-Si interface states density have been determined by the admittance spectroscopy. The performance of the cell has been found to be

limited by the detrimental interface defect states at the MoO_x/n-Si interface (~2×10^{12} eV^{-1} cm^{-2}), along with high n-Si/LiF_x back-surface recombination that has reflected in quantum efficiency response in the longer wavelength region (800 nm to 1100 nm). The presence of a large number of interface defect states at the MoO_x/n-Si junction result weak inversion layer and high reverse saturation current density of ~4.1×10^{-8} A/cm^2.

Process and configuration dependent Ag/ITO/MoO_x/n-Si/LiF_x/Al CSC silicon solar cells having conversion efficiencies from 6.5% to 14.5% have been investigated. Some of the cells' anomalous characteristics in light J-V and Suns-V_{OC} graphs have been analysed by photo-induced capacitance-voltage (C-V), impedance spectroscopy (IS), and voltage- plus light-biased (white, blue and infrared) quantum efficiency (QE). Correlated analysis of cells has revealed the physical origin of S-shape in light J-V and turnaround in Suns-V_{OC} graphs. After air exposure of the MoO_x film, the charge carrier accumulation at the front interface and inefficient transport through the MoO_x layer have led to the anomalous features in light J-V and Suns-V_{OC} graphs of the cell. This is reflected as an additional peak and arc in C-V and IS graphs, respectively. In the absence of the LiF_x layer, the cell has shown the only turnaround in Suns-V_{OC} graph due to the Schottky barrier. The IS analysis resolved carrier transport issues at the front junction and back contact of the cells with a distinguished response. The light-bias dependent QE analysis has confirmed the presence of carrier collection barrier at the MoO_x/c-Si interface, and the Schottky contact at the back with a different response in the cells' EQE spectra.

The CSC silicon heterojunction solar cells have been fabricated using Nickel Oxide (NiO_x) as a hole-selective layer by thermal evaporation. The highest power conversion efficiency of ~15.20% with the chemically grown SiO_x interlayer has been achieved from Ag/ITO/NiO_x/n-Si/LiF_x/Al cell structure in comparison to ~12.43% without SiO_x. The cells without and with SiO_x layer have been analyzed by considering crucial parameters for conversion efficiency like; minority carriers' diffusion lengths, lifetimes, recombination

resistance, the density of interface defect states at the NiO_x/n-Si junction; by studying the dark/light current density-voltage, quantum efficiency, impedance and parallel conductance characteristics. The device analysis has given evidence for cell's open-circuit voltage and short-circuit current enhancement with the SiO_x interlayer. This is due to an improvement in minority carrier lifetimes from ~8.6 µs to ~48.27 µs (photo-conductance decay analysis), which is also estimated from ~7.45 µs to ~49.20 µs by impedance spectra analysis, minority carrier diffusion length from ~171 µm to ~952 µm and decrease in rear surface recombination velocity from ~1106 cm/sec to ~170 cm/sec (Quantum Efficiency analysis). These investigations have revealed that engineering the n-Si/LiF_x interface by the SiO_x interlayer is more critical than the NiO_x/n-Si interface for device performance enhancement, since, thin unintentionally grown SiO_x layer during NiO_x evaporation simultaneously mediating silicon surface passivation.