Thesis Title:

Low Frequency Noise Characterization and Modeling of Advanced CMOS Devices

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Abstract:

The relentless demand for high-speed processing and improved integration in modern electronic systems has compelled device engineers to pursue aggressive scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs). This downscaling has led to remarkable improvements in transistor performance and speed, achieved by reducing the geometric dimensions of these devices and substituting conventional material combinations with newer, superior alternatives. However, the advantages of scaling down are accompanied by considerable challenges, as various short-channel effects (SCEs) start to emerge. Key SCEs such as threshold voltage roll-off, drain-induced barrier lowering (DIBL), and punch-through start to affect device behaviour, presenting obstacles to achieving optimal performance.

One critical challenge that arises from continued scaling is the increase in low frequency noise, particularly flicker noise ($1/f$ noise). This type of noise is intrinsic to the operation of MOS devices and tends to scale with the shrinking dimensions of the transistors. As device sizes are reduced, flicker noise becomes more prominent and poses a serious limitation to the performance of MOS devices, especially in high-precision and low-power applications. Moreover, $1/f$ noise becomes even more critical at cryogenic temperatures, a regime essential for quantum computing applications. The precise control and reduction of this noise at extremely low temperatures is a major concern for researchers aiming to optimize devices for quantum computing, where noise can disrupt quantum coherence.

This thesis focuses on an in-depth investigation of flicker noise in advanced CMOS (complementary metal-oxide-semiconductor) devices. By performing detailed characterization, thorough analysis, and advanced modeling techniques, the study aims to uncover the complexities of flicker noise to enhance understanding and explore its potential applications. To achieve this, comprehensive characterization and analysis are conducted on on-wafer partially depleted silicon-on-insulator field-effect transistors (PDSOI FETs), bulk FETs, and bulk fin field-effect transistors (FinFETs) across a wide temperature range, from 300K to 10K. The study also investigates how scaling affects flicker noise in MOS devices. In

addition, the impact of hot-carrier degradation on flicker noise in 45-nm node PDSOI FETs are explored, offering key insights into the reliability concerns related to this noise phenomenon. Furthermore, low-temperature compact modeling of CMOS devices is achieved by enhancing industry-standard BSIM (Berkeley short-channel IGFET model) models with additional equations in Verilog-A, allowing for more accurate simulation of DC and $1/f$ noise behaviour at cryogenic temperatures. The modeling of thin and thick oxide MOSFETs using commercial process design kits (PDK) is also presented.