Abstract

The present-day need to handle extremely complex computational problems efficiently and the promising results that quantum computers have demonstrated in this regard has catered attention of the researchers in the quantum computing domain. To achieve the targeted Noisy Intermediate Scale Quantum Computers (NISQ), researchers have been investigating the possible innovative solutions to address the current qubit scale-up challenge. The most promising solution that has emerged is the monolithic integration of qubits and control electronics in silicon, paving the path towards Quantum Integrated Circuits (QICs), which requires qubits and cryo-electronics to be operated at ∼1K to 4K temperature.

Research reports from the past have focused on the investigation and to some extent, modeling of planar bulk CMOS and 22nm FDSOI technology for cryogenic electronics applications. This thesis is targeted at cryogenic investigation of sub-10nm FinFETs and PDSOI devices, and the cryo-compatible industry standard compact models that comprehensively capture the low temperature physics using the most efficient semi-empirical equations. Detailed characterization and analysis of these advanced technology node devices has been done from 300K down to 10K temperature. The temperature trends for transfer and output characteristics; focusing on various electrical parameters such as threshold voltage, subthreshold swing and mobilities; are studied and the plausible underlying physical phenomena have been comprehended. Extensive experimental investigation of electron and hole mobilities in n- and p-channel FinFETs has been presented from 300K to 10K for variable geometry devices. It is found that short-channel FinFETs show mobility degradation that jeopardizes the cryogenic benefits. Further, multifrequency capacitance and conductance behavior of these devices has been evaluated to understand the effect of frequency coupled with cryo-temperatures on interface defects/traps, series resistance, dielectric response time and the tunneling currents.

After a detailed study on FinFETs, the impact of cryogenic temperature on the performance of SOI technology is evaluated. For SOI, self-heating due to the presence of thermally isolating BOX layer is a major concern. Thermal behavior of the 45nm PDSOI devices has been examined at cryogenic temperatures. Due to the reduced thermal conductivities at cryogenic temperatures, aggravated self-heating

effect is observed at low temperatures. Another major issue with PDSOI devices is the memory effect due to floating body charge instability, which has also been extensively addressed in this thesis.

The industry-standard compact models have been used over the years for commercial applications. With the advent of cryogenic applications of CMOS devices, these models need to be extended for these cryogenic effects. Hence, this thesis also presents a unified compact model that can be used to predict MOS device characteristics from room temperature down to cryogenic temperature by proposing modifications to BSIM-CMG and commercial PDKs. The circuit-level simulations are performed at cryogenic temperatures to understand the circuit implications of the low-temperature effects and to test the applicability of the proposed models.