ABSTRACT

This thesis investigates two-switch based buck-boost converter topological evolution and their performance improvement aspects. To improve the voltage transformation ratio of the conventional buck-boost converter, a new family of two-switch based double buck-boost gain converters (DBBGC) are evolved. The basis for the topological evolutions of the DBBGC converters is parallel-input series-output connection of the buck-boost and SEPIC converters. This evolution resulted in three different topologies exhibiting double buck-boost voltage gain along with reduced current ripples. These topologies are named as DBBGC Type-1, DBBGC Type-2 and DBBGC Type-3. Detailed mathematical analysis is established to identify the performance aspects. Through time-domain analysis, voltage and the current stress associated with the circuit components are derived. Furthermore, the state-space models are formulated by using equivalent circuit analysis to design the suitable controller and understand their dynamic behaviour under closed-loop operation. A comprehensive study between the proposed DBBGC converter topologies and reported buck-boost topologies is discussed to bring out the effectiveness of the proposed DBBGC converters. The functionality of DBBGC converters is demonstrated through simulation and experimental measurement results. Amongst these, the proposed DBBGC Type-3 exhibits low output capacitor current ripple due to the presence of an inductor at the load side.

The three proposed DBBGC converters exhibit improved voltage transformation ratio as compared to the conventional buck-boost converter but the current ripple in the source side is little high. Also, there is no common ground between the source and load ports. To eliminate some of these shortcomings, another class of two-switch based quadratic buck-boost gain converters (QBBGC) are proposed. The basis for these evolutions is cascading of boost converter followed by the restructured ZETA converter. Direct cascading of boost converter with ZETA converter yields a pseudo quadratic conversion ratio and an additional buck stage is mandatory to transform the gain to quadratic buck-boost gain form. To realize the quadratic buck-boost voltage transformation without adding additional stages, a modified boost configuration at the front-end together with re-structured cascading approach is adopted in the topological evolution. This evolution resulted in three different topologies exhibiting quadratic buck-boost voltage gain named as QBBGC Type-1, QBBGC Type-2 and QBBGC Type-3. The proposed QBBGC topologies exhibit minimal current ripples like in CUK converter along with common grounded structure over the existing QBBGC configurations. The steady-state and state-space analysis is presented for QBBGC converters. Also, a comprehensive performance review is formulated for ready reference and comparison. The steady-state and load voltage regulation features of QBBGC topologies is demonstrated through simulation and experimental measurement results.

The proposed QBBGC converters have improved voltage transformation ratio features as compared to the proposed DBBGC converters but the boosting duty cycle range is not very wide. Additionally, the voltage stress associated with the upstream side power devices is higher than the output voltage in the proposed QBBGC topologies. In an attempt to extend the boosting range operation along with low voltage stress on the upstream side power devices, three two-switch based extended boosting range buck-boost converter (EBRBBC Type-1, Type-2 and Type-3) topologies are evolved. The capacitor-diode cell is embedded on either sides of the conventional quadratic buck-boost converter while formulating the Type-1 and Type-2 topologies. EBRBBC Type-3 converter topology is formulated through the cascading of boost converter followed by modified inverting boost converter. Salient features offered by these topologies are: (i) continuous input current profile with low ripple content, (ii) low voltage stress on power devices and (iii) common ground between source and load. The mathematical analysis of the steady-state voltage and current relations of the passive and active components are derived using the time-domain approach for the proposed EBRBBC converters. Detailed time-domain and state-space analysis is established for these EBRBBC topologies by using network analysis. Thereafter, a comprehensive performance review of these EBRBBC converter topologies is discussed. The performance features are validated through illustrative simulation and experimental measurements.