TCAD Based Modelling of Line-Edge-Roughness and Radiation Effects in Advanced CMOS Devices

Abstract

CMOS scaling became popular among researchers and the semiconductor industry since it provides many advantages like faster speed, higher performance, and increased integration density on a chip. Despite the above advantages, short channel effects are a major concern for planar devices at lower technology nodes which led to the development of multiple-gate FETs (MugFET), such as Nanosheet FETs (NSFET), Nanowire FET (NWFET), and FinFET as a replacement for planar MOSFETs. Among all these MugFETs, for sub-7nm technology node, NSFETs are a potential replacement of FinFET and NWFETs due to their high drive current and speed. However, the small channel area and doping profile make these MugFETs more susceptible to Process induced variation. In this thesis, some of these issues are discussed and solutions are proposed. The work presented in this thesis is done using Synopsys Sentaurus TCAD and all the characterization is done using Cascade manual prober along with Keysight B1500 parameter analyzer. In the initial part of the thesis, CMOS FETs are designed and simulated using Sentaurus TCAD to match Semiconductor Laboratory (SCL) CMOS 0.18µm device's physical design and electrical characteristics. Id-Vgs of n and p-type FETs are measured in linear as well as in the saturation region and finally calibrated using the Sentaurus TCAD model. SOI device's faster speed, resistance to latch-up, and immunity against radiation make it preferable over conventional planar devices. PD SOI and FD SOI FETs are also designed to a specific 0.18um CMOS target using a calibrated TCAD model for radiation analysis.

MugFETs with small channel area are subject to Line edge roughness (LER) due to process-induced variation. LER can result in a high mismatch in FET's

electrical characteristics. In this thesis, a 3-D LER model has been taken for the accurate analysis of mismatch in NS and NW-FETs electrical characteristics. The mismatch performance of NSFET is investigated and reported for different NS widths. Also, SCE performance parameters, like DIBL (mV) and SS (mV/dec) sensitivity to LER are investigated in this chapter. Moreover, the Junctionless mode devices (JL) are preferred over Inversion mode (IM) devices for nanoscale FETs design due to their simple fabrication process, high drive current, and feasibility of doing short channel length design. However, JL FETs are more susceptible to process-induced variation. This thesis also includes a study of matching the performance of inversion (INV) and junctionless (JL) NS/NW-FETs devices for 3-D LER.

Semiconductor devices are also being widely used in space for various applications, also affected by the presence of Cosmic rays consist of different particles such as heavy-ions, neutrons, protons, electrons, alpha particles, and gamma rays. Among these cosmic ray particles, heavy-ions cause a change in the state of memory element or temporary circuit failure due to instantaneous transient current spike in devices. In the next part of the thesis, heavy-ion induced single event transient (SET) in bulk and SOI NSFET are discussed. Vertically stacked nanosheets are designed and simulated using the inbuilt heavy-ion Sentaurus TCAD model. SET current in bulk and SOI NSFETs for different device dimensions are investigated and discussed in this thesis. Also, the effect of the different angles of ion incidence on SET performance is analyzed. SOI NSFETs show a distinct advantage over bulk devices for heavy-ion SET. Further, different 3-D SOI MugFETs, such as FinFET, NSFET, and NWFET are simulated for SET due to heavy-ion irradiation and compared. Finally, an empirical model is also presented in this thesis to predict the SET current with physical design parameters of MugFETs, and as well as the heavy-ion model parameters. Physical design as well as heavy-ion parameters, such as nanosheet fin width/ thickness, the diameter of a nanowire, linear energy transfer (LET),

angle of incidence, and channel doping are incorporated to accurately predict SET due to heavy-ion irradiation on these MugFETs.