The continuous scaling down of semiconductor technology has helped achieve low-power and low-cost image sensors. The reduction in pixel pitch has improved the resolution of the image sensors. However, the reduction in the pixel pitch due to technology scaling has made it difficult to achieve high full well capacity (FWC) and high dynamic range while maintaining high resolution. Achieving high sensitivity and high resolution while maintaining high dynamic range requires accurate and efficient estimation of the FWC of a four transistor (4T) pixel in a CMOS image sensor (CIS). The FWC of a 4T pixel depends on the pinned photodiode (PPD) capacitance, pinning voltage, potential barrier, temperature, and operating voltages. Thus, it is inevitable to understand and model the fundamental characteristics of a 4T pixel in a CIS. The thesis primarily focuses on the simulation and characterization-based studies of 4T pixels for dynamic PPD capacitance and barrier modulation in CIS. In this thesis, an analytical model for the PPD capacitance is derived. The proposed model relies on the total current flowing through the PPD in low and high illumination conditions. The proposed model is further elaborated due to barrier modulation observed in the transfer gate (TG) channel at the PPD-TG interface in the absence and presence of a potential pocket. Understanding the potential changes in PPD, PPD-TG interface, and TG channel as a function of integrated PPD charges is a complex problem and needs a detailed analysis. The model is evaluated for light intensity, integration time, temperature, and transfer gate voltage values. The model is validated with technology computer-aided design (TCAD) simulations. The PPD capacitance model is validated experimentally by estimating the feedforward charges at the floating diffusion node, collected due to thermionic emission current. The non-linearity observed in the feedforward voltage is also explained using the non-linear behavior of TG channel potential. The non-linear behavior of TG channel potential influences the effective potential barrier, thereby influencing the FWC and PPD capacitance. Further, the barrier modulation study is extended by discussing the influence of interface traps in the charge transfer path. The interface traps influence the potential barrier differently when PPD is in the dark than when illuminated. The study will help better understand FWC, feedforward charges, and dark current generation mechanisms in a PPD. The results presented in the thesis can be a resource for CIS pixel designers to analyze, simulate, and optimize a 4T pixel.