Abstract

In the current era of Noisy Intermediate-Scale Quantum (NISQ) based quantum computers, as many as 1121 qubits can be integrated into a single Quantum Processing Unit (QPU). However, for these quantum computers to be used as general-purpose computers solving complex problems, the number of qubits in a QPU must be in millions. To achieve this milestone, the use of industrial CMOS platforms is increasingly being proposed as a feasible alternative. The industrial CMOS platforms offer tight packaging densities, small on-wafer footprints and excellent control over the geometry of the fabricated devices, which can, in principle, allow large-scale integration of thousands of qubits into a small QPU volume. However, as the physics behind the operation of quantum devices in QPU differs drastically from the operation of classical FETs, the design of quantum devices in the industrial CMOS platform has been extremely challenging.

To help circumvent this problem, the presented thesis showcases how an industrial short channel FinFET, designed in 10-12 nm technology node can be used to realize quantum devices of a QPU such as Single Electron Transistors (SETs), Quantum Dot Thermometers (QDT), Coulomb Blockade Thermometers (CBTs) operational at cryogenic temperatures. Results show that the cryogenic operation of these industry standard short channel FinFETs operating at its subthreshold bias regime leads to the formation of a gate-defined Quantum Dot (QD) in the channel, which is electrostatically confined by the potential barriers in the Lightly Doped (LDD) region of the channel just below the gate spacers. The small channel volume of these FETs allows the channel's QD to have extremely small spherical equivalent diameters (10 to 15 nm). This allows these devices to work in QD / Quantum mode for temperatures as high as 40 K, where only a handful of quantum devices have been reported to be operational. The quantum mode of operation in these devices thus allows them to be used as a CMOS-friendly alternative to traditional non-CMOS processing-based large-footprint devices such as SETs, QDTs, CBTs, and qubits commonly used in a QPU.

The performance of these industrial FinFETs operating at 8 K is comparable to the state-of-the-art quantum devices operated at much smaller cryogenic temperatures (10 mK). Moreover, as these proposed FinFET based QD devices can be operated at relatively higher cryogenic temperature stages (above 7.8 K) where the thermal

cooling capacity of the cryogenic hardware is sufficiently large, a large scale QPU volume can be realised/tolerated within the thermal budget of the cryogenic cooling assembly.

Although the QD-based operation in the cryogenic FinFETs is distinctive for a small gate bias range, experimental results show that the variation in the Number of Fins and/or Threshold voltage enables the precise tuning of the gate bias range in which the QD-based operation is desired to be operated. The impact of other geometry-dependent parameters, such as the Number of Fingers, masked gate length, and channel type (p-type and n-type) on the properties of the channel's QD is explored in grave detail. This geometry-dependent study is expected to serve as a rule book for any CMOS device engineer to help build QD-based devices using these FinFETs. The QD size is also found to be highly uniform across identical geometries of FinFETs, which helps further advocate the precise control of the QD properties offered by these industrial CMOS platforms.

To help feasibly design and validate the operation of these FinFET based QD devices before its physical fabrication, a Verliog-A based compact model is proposed. The proposed model is built on top of the BSIM-CMG compact model and accurately captures the classical performance and quantum performance of these FinFETs across the wide dynamic temperature range of 300 K down to 8 K. The proposed model can be used to design the cryogenic-CMOS-based control and readout electronics of a co-integrated QPUs. The model helps evaluate the performance of Hybrid SET-FET circuits built entirely using the proposed FinFETs. The challenges with such full-CMOS-based design of hybrid circuits and their solutions are discussed in grave detail to fully comprehend the design prospects with these new FinFET-based QD technologies.

COMSOL multiphysics simulations of the QD performance in FinFETs operating at cryogenic temperatures are also presented in this work to showcase how the body bias can be used to fine-tune the charge sensitivity of the QD formed in the channel. A compact modeling framework for the simulation of a silicon spin qubit is also presented to help simulate simple quantum-gated operations in popular stimulative platforms such as MATLAB.