Abstract of Ph.D. Thesis

"Integrated mm-Wave Receiver Components for Low-Power Applications"

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The primary focus of the proposed thesis is on the design and implementation of integrated mm-wave receiver components for low-power. The receiver components consist of an on-chip antenna, a low-noise amplifier, and a quadrature voltage-controlled oscillator. The on-chip antenna is designed and fabricated in a 180 nm CMOS process, and the LNA is designed and fabricated in a TSMC 65 nm CMOS process. The LNA and QVCO are designed for low power consumption.

This work is divided into three parts: the first one discusses the on-chip CMOS antenna, the second one discusses the 36 GHz LNA, and the third one discusses the two QVCOs, one at 36 GHz and the second one at 60 GHz frequency of operation. Two patch antennae are discussed at a nominal resonance frequency of 77 GHz, namely a thin-substrate antenna and a thick-substrate antenna, using a standard 0.18 μm CMOS technology. Both the antennae are implemented on metal-6. The thin-substrate antenna uses metal-5 as the ground plane, and the thick-substrate antenna uses metal-1 as the ground plane. The thin-substrate antenna was fabricated on a 0.18 μm CMOS process and characterized. The thick-substrate antenna was only simulated. Measurements of the thin-substrate antenna show a peak S_{11} of -18.22 dB at 99.8 GHz. In the simulation, the thin-substrate antenna has a peak gain and radiation efficiency of -25 dB and 1%, respectively, at 77 GHz. The thick-substrate antenna has a simulated peak gain and radiation efficiency of 5.18 dB and 58.31%, respectively, at 77 GHz.

The second part presents G_m boosted CG$-$CS low power, high gain LNAs for 5G applications. The LNA is cascaded with a CG cascoded stage and a CS cascoded stage. In the first stage, a transformer-based gm boosting technique has been used along with series peaking. The second stage is used to increase the gain in total. The two LNAs are discussed: the Single Stage LNA and the Two Stage LNA. Both the LNAs are designed and fabricated in the TSMC 65 nm CMOS process. The single-stage LNA measured results show a gain of 9 dB and a noise figure of 4.1 dB. The minimum NF obtained is 3.8 dB at 36.2 GHz and is below 4 dB from 33 GHz to 37 GHz.The proposed LNA consumes only 4 mW from a 1-V supply.

The third part presents two QVCOs, one at 36 GHz and the second at 60 GHz. The first one is a 36 GHz quadrature voltage-controlled oscillator (QVCO) designed and fabricated with a transistor coupling mechanism that uses only one single-turn ring inductor. The second QVCO is a 60 GHz transformer-coupled low-power quadrature voltage-controlled oscillator (QVCO), also designed using a single-turn ring inductor. The single-turn inductor is shared by the pair of oscillators in both the QVCOs. A digital cap bank is used for fine-tuning the oscillator. The circuit is designed in a 65 nm CMOS process. The frequency of the oscillator is tuned from 59.5 to 60.5 GHz.

The proposed 60 GHz QVCO exhibits a phase noise of -81 dBc/Hz at 1 MHz offset frequency. The DC power consumption is 3.3 mW with a supply voltage of 1 V.

KEYWORDS: RFIC, Fifth generation millimeter wave (5G mmWave) communication systems, 36-GHz, 60 GHz, 77GHz, receiver (Rx), low noise amplifier, mmWave, QVCO, On-chip antenna