On-Chip Instrumentation Techniques

Abstract

Integrated circuits today are built to function at very high frequencies due to the improvement in signal processing bandwidth achieved. Systems such as processors, transcievers, memory sub-systems are designed in extremely scaled-down processes with very fine time resolution to operate at GHz frequencies so as to perform fast and complex functions. This prompts a need for us to build instrumentation systems that can accurately characterize the performance of these complex systems-on-chip. Circuits that are used to probe internal nodes and expose them to pads can degrade the actual performance of the systems, hence triggering a possibility of over-design. This work aims to explore instrumentation systems that can be used for characterization on-chip so that all sensitive performance measurements can be done in-situ. The most preliminary measurements required for accurately estimating performance are voltage, current and time. Multiple systems have been proposed in this work to enable on-chip measurements.

Measuring voltages and currents on a chip requires a reference voltage. In this work, we propose an ultra low power portable reference integrated regulator that can also support upto 10mA of load current. This system was designed in a TSMC 180nm bulk CMOS process and was able to achieve a temperature stability of 80 $ppm/^oC$ with a core current consumption of 187 pA.

Another suitable candidate for on chip measurement is time and its derivatives, primarily frequency, rise time, fall time etc. To enable these

measurements, we propose a state-learning fractional frequency synthesizer with built-in spur reduction. This algorithm is tested using an FPGA development board, discrete DAC and VCO chips. This prototype is used as a proof of concept to show a frequency synthesizer that is fast sweeping (useful for spectrum and s-parameter measurements).

As the PLL works to control the phase noise spectrum within its bandwidth, a VCO with a good spectrum at frequencies outside the bandwidth of the PLL. We propose a new VCO architecture designed at 5GHz that has a figure of merit better than $-200\ dBc/Hz/mW$.The inductors were custom designed and characterized using EMX to achieve better quality factor for the required frequency of operation. The entire VCO with the additional startup oscillator is designed in the TSMC 65nm LP process. The VCO core consumes about 7mA from a 1.2V supply and has a phase noise of $-132\ dBc/Hz$ at a 1 MHz offset.

A common method of observing periodic high frequency signals in the time-domain is by using a sub-sampling oscilloscpe. To enable this, we propose a sub-sampling front-end with a low input load of 12 fF followed by a second order continuous time delta sigma ADC. The ADC achieves an approximate ENOB of 12 bits in post-layout extraction and the front-end can track and hold signals upto few GHz.