

Title: CARRIER-SELECTIVE CONTACT SILICON SOLAR CELLS: ROLE OF SILICON SURFACE MORPHOLOGY AND AGEING ON DEVICE PERFORMANCE

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ABSTRACT

In this thesis work, the performance of carrier selective contact (CSC) based silicon solar cells is mainly explored. The solar cells are fabricated at room temperature on industrially feasible silicon wafers. In these solar cells, the silicon surface plays a vital role in achieving high device performance efficiency. To investigate the effect of silicon surface on a device performance, CSC solar cells are fabricated on different pyramids size textured surface. For the average pyramids size of 2, 5, and 8 μm , the τ_{eff} values are 126, 95, and 65 μs respectively, which after the CP treatment are 154, 130, and 99 μs , respectively i.e., an absolute increase of $\sim 30 \mu\text{s}$ is observed in each case.

The enhancement in τ_{eff} value is noted due to smoothing of pyramid peaks/valleys. The role of silicon surface is also verified on room temperature fabricated CSC solar cells having structure Ag/ITO/MoO_x/n-Si/LiF_x/Al, where MoO_x and lithium fluoride (LiF_x) work as hole- and electron- selective layers, respectively. Though the cell fabricated on small pyramids ($\sim 2 \mu\text{m}$) has shown better performance efficiency of $\sim 14.53\%$, after the CP treatment, not much efficiency variation is observed. However, the CP treatment is useful for medium/large pyramids ($\sim 5-8 \mu\text{m}$) based cells, which has improved the open-circuit voltage (45-63 mV) after smoothing/rounding of sharp pyramid peaks/valleys. The reduction in photocurrent is observed due to an increase of light reflection from smoothed pyramid surfaces. Quantum efficiency along with reverse saturation currents analysis have provided better insight into understanding

the silicon surface passivation, MoO_x/n-Si junction quality, and low-barrier shunts present at the pyramid peaks/valleys.

Further, the crystalline silicon (c-Si) surface passivation has been explored with sputtered hydrogenated intrinsic amorphous silicon (S-i-a-Si:H) and thermally evaporated molybdenum oxide (MoO_x) layers. For analyzing the passivation quality of c-Si surface, temperature- and injection-dependent lifetime spectroscopy (TIDLS) technique has been adopted. The analysis is based on the parameters such as the minority carrier effective lifetimes (τ_{eff}), the activation energy of surface/interface defect states (ΔE), and the electron to hole carrier capture cross-sections ratio (k) at the interface. The S-i-a-Si:H passivation layer has shown τ_{eff} of $\sim 70 \mu\text{s}$ and ΔE of $\sim 51 \text{ meV}$. However, MoO_x films have been revealed with the τ_{eff} of $\sim 110 \mu\text{s}$ and ΔE of $\sim 109 \text{ meV}$. The S-i-a-Si:H layers are incapable of minimizing the c-Si surface trap states with the chemical passivation of dangling bonds due to the creation of additional surface defect states by the sputtering damage. To compare the passivation quality, the silicon wafer is separately passivated by plasma-enhanced chemical vapour deposited i-a-Si:H films, and the estimated defect energy levels are $\sim 86 \text{ meV}$ and $\sim 39 \text{ meV}$ with much better temperature-dependent lifetime response. The passivation mechanism of the sputter and PECVD deposited i-a-Si:H are analyzed using FTIR spectroscopy with respect to the chemical bonding and level of hydrogenation from the two techniques. Entirely different defect energy level positions from the sputter passivated silicon surface (compared to the PECVD sample) has provided evidence of sputtering damage to silicon surface from high energy ions in the plasma. However, the MoO_x layers have shown better passivation because of reduction of majority carriers by the carrier inversion (field-effect passivation) and chemical passivation.

Further, the stability of the CSC solar cells (Ag/ITO/MoO_x/n-Si/LiF_x/Al) have been investigated based on silicon surface morphology (planar, different pyramid sizes, and

chemical polishing of pyramids). The stability of the device on small silicon pyramids ($\sim 2 \mu\text{m}$) is better with time than the medium/large pyramids ($\sim 5 \sim 8 \mu\text{m}$). The chemical polishing of pyramids has minimized the microstructural stress (tensile in the valleys and compressive at the peaks), which further improved the stability of cells with ageing, which has been also verified indirectly with cells fabricated on a planar surface. The degradation of performance of the cell based on the silicon surface morphology has pointed out the instability of the MoO_x layer and Schottky barrier reduction, which produces a barrier to hole-transport at the $\text{MoO}_x/\text{n-Si}$ junction with the S-shape in J-V graphs under illumination. The ageing effect on the performance degradation is further explored using the Sentaurus TCAD simulations with the MoO_x layer work function variation, and the study specifies the band bending reduction (minimal carrier inversion) and hole transport barrier at the junction region.

Further, numerical simulation of CSC solar cells ($\text{Ag/ITO/MoO}_x/\text{n-Si/LiF}_x/\text{Al}$) has been performed based on the experimental data using an industrial quality base silicon wafer by the Sentaurus TCAD software. The role of (1) electron-selective LiF_x layer and its thickness, (2) hole-selective MoO_x work function variation, and (3) front contact ($\text{MoO}_x/\text{n-Si}$) surface passivation interlayer has been explored on the device performance. The LiF_x layer at the rear side has provided an electrical barrier to the minority carriers (holes), which led to the enhancement in device photocurrent and a slight improvement in open-circuit voltage. The thickness of the layer controls the efficient extraction of the majority carriers (electrons). The work function of MoO_x layer is crucial for modifying the induced strong inversion layer with better built-in potential at the $\text{MoO}_x/\text{n-Si}$ interface to attain high open-circuit voltage. A thin SiO_x interlayer passivation layer at the $\text{MoO}_x/\text{n-Si}$ interface has significantly improved the device's open-circuit voltage by minimizing the minority carrier recombination at the interface.