Abstract

Index Terms: SiC MOSFET, SBD, double-pulse test, half-bridge, parasitic inductance, parasitic capacitance, reverse recovery, switching loss, junction temperature, analytical loss model, calorimetric measurement, on-state voltage measurement active thermal control, inverter-based resource.

SILICON carbide MOSFETs are increasingly being accepted in the power electronics sector because of their exceptional physical and electrical properties, allowing them to function at higher switching frequencies. The increased switching transition rate and higher switching frequency of the SiC MOSFETs result in a greater influence of the circuit's parasitic elements on the switching profiles, leading to a considerable impact on the switching losses. Hence, precisely estimating the switching losses continues to be a challenging task. Further, loss estimation often aims to find the safe operating limit for power semiconductor devices as it remains the major design limitation; therefore, this also necessitates a simple yet accurate thermal model to estimate the junction temperature.

Therefore, this thesis begins with the motivation for modelling the switching loss of the SiC MOSFETs. Two often employed bridge leg configurations in the field of power electronics are the Diode-MOSFET and MOSFET-MOSFET structures, and this thesis primarily focuses on the later arrangement for developing a loss model based on the datasheet parameters to estimate temperature-dependent switching losses due to the impact of the reverse recovery charge of the anti-parallel body diode of the SiC MOSFETs. In addition, the developed model considers the parasitic components' effects, allowing for a comprehensive knowledge of the switching characteristics of the SiC MOSFETs in various operating conditions. Subsequently, the accuracy of the proposed loss model has been verified by comparing its result with the state-of-the-art double pulse test and calorimetric test results.

In terms of junction temperature estimation, direct measurement is not practical, and indirect non-invasive methods such as temperature-sensitive electrical parameters-based measurement techniques require substantial effort in building and calibrating the sensing circuits. Therefore, an electro-thermal model has been de-

veloped, where an RC network-based thermal model has been implemented, which takes the power loss data from the developed loss model and iteratively returns the junction temperature. The effectiveness of the proposed method has been demonstrated by comparing its results with the conventional and on-state drain-source voltage measurement-based TSEP estimation techniques on a 10kW three-phase interleaved boost converter.

Subsequently, the opportunity to increase the kVA limit of a power electronic converter without breaching the safe operating limit of the junction temperature through the active thermal control technique has been explored. Wherein the applicability of the earlier discussed electro-thermal model for active thermal control is also shown. In the presented active thermal control approach, a discontinuous pulse width modulation strategy, which controls the bus clamp angle according to the virtual junction temperature feedback for increasing the kVA limit of the grid-connected inverter-based resources, is discussed. The impact of a system-level current controller for the kVA increment has also been briefed. Additionally, the effect of DPWM on switching losses P_{sw} is shown by establishing an analytical relationship between the bus clamp angle with respect to switching loss.

In conclusion, the main contribution of the thesis regarding temperature-dependent loss modelling, junction temperature estimation, and control through active thermal control techniques for SiC converters is summarised, and a brief outlook on possible future research work is discussed.