ABSTRACT

Two quadratic following boost converter (QFBC) topologies are evolved with voltage gain trend following the conventional quadratic boost converter (QBC). Both these topologies are capable of realizing high voltage gain at trade-off duty ratios. Detailed mathematical analysis is established to bring out salient features of the proposed QFBC topologies. Both these topologies have similarity as their gain variation closely follows the conventional quadratic boost converter. The QFBC Type-1 topology gain is slightly lower than the conventional quadratic boost converter while QFBC Type-2 exhibits a little higher gain. QFBC Type-1 has lesser voltage gain sensitivity and control complexity than traditional QBC whereas QFBC Type-2 has lesser capacitor voltage stress than the conventional QBC. Quadratic following voltage gain features and other steady-state performance aspects of the proposed topologies are verified through experimental investigations. Detailed state-space analysis is established for both the QFBC topologies and control-to-output plant along with other transfer functions are formulated. Subsequently, these transfer functions are used as plant models to design the robust controllers.

After topological evolutions, suitable controller selection and design aspects to achieve load voltage regulation are investigated. Closed-loop stabilization of the proposed topologies is carried out using the single-loop and double-loop voltage-mode control strategies. In case of single-loop voltage-mode control, a proportional plus integral plus derivative (PID) controller structure is adopted. Proportional plus integral (PI), proportional plus derivative (PD) controller combinations are adopted for the double-loop voltage-mode control scheme. These controllers are designed such that the proposed QFBC topologies reliably operates while delivering the desired voltage boosting ratios. To achieve this, the designed single-loop as well as double-loop controller configurations must be ensure robustness and performance specifications. In this context, firstly stabilizing region for the controller parameters is generated using stability boundary locus approach. Thereafter, controller parameter region is squeezed by adding (i) Kharitonov polynomials based constraints to handle the plant uncertainties and (ii) relative stability performance quantification constraints: gain margin and phase margin. Final controller
parameters are chosen from this region based on minimum integral error index and for PID controller it is inversely proportional to the maximum value of the integral constant.

It is easy to deal with parameter uncertainty using Kharitonov polynomials but the resultant controller parameter stabilizing region is conservative and hence controller performance may not be guaranteed. Moreover, for the QFBC topologies (which are non-minimum phase systems) it is difficult to achieve desired performance and robustness range using single-loop voltage-mode control scheme alone. In an attempt to enhance the performance and robustness aspects of the proposed QFBC topologies, a double-loop voltage-mode control strategy is proposed in this thesis. Though this double-loop controller works by using load voltage information only and yet its performance is close to two-loop control scheme (i.e. inner current-loop and outer voltage-loop). On the basis of parameter-space approach, firstly the stabilizing regions in the controller parameter plane are generated. Thereafter, these stabilizing regions are squeezed upon enforcement of robustness and performance related constraints which are: (i) absolute stability criterion, (ii) the guaranteed combined sensitivity and (iii) guaranteed up-down glitch margin. From this region, the final robust controller parameters are chosen based on 'fmincon' solver based constrained optimization. Integral time square error (ITSE) performance index is used for optimization. Though this controller is sufficiently robust but there is no guarantee that it ensures performance quantification such as settling time and overshoot. With performance realization being the prime consideration, generation of double-loop voltage-mode controller parameter stabilizing region which ensures guaranteed dominant pole region is investigated. Like in single-loop voltage-mode controller, here also ITSE performance index along with constrained optimization is used to obtain the final controller which ensures settling time and overshoot requirement. The efficacy of single-loop and double-loop controllers for closed-loop stabilization of quadratic following boost converter topologies are verified experimentally. Controllers effectiveness in terms of load voltage regulation, disturbance rejection, reference tracking, ensuring settling time and overshoot requirements are also demonstrated experimentally. Also to highlight double-loop voltage-mode controller performance improvement, dynamic responses are compared and illustrated with the PID controller dynamic performance characteristics.