RF FRONT-ENDS FOR ASYNCHRONOUS TRANSCEIVERS

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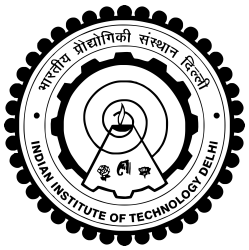

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Abstract

Wireless Sensor Networks (WSN) covers the broad area of applications that may be bio-medically inspired, commercially inspired, or maybe needed for military applications. Specifically, the bio-medically inspired body-area WSN have a fundamental requirement of low power consumption, moderate data rate, and microscopic volume. For applications like capsule endoscopy, intra-ocular transmitters, pacemakers, and neural recorders, the entire system is to be packaged with minimal volume. As such, in such applications, there is no room for a discrete crystal oscillator. Also, minimum power should be consumed during the data transmission to maintain the communication link for a more prolonged period until capsule travels entirely through the large and the small intestine, which takes approximately 24 hours. However, a moderate to high data rate is required to maintain the picture quality. These specifications are mostly dictated by the application leading to the specific transceiver architecture design.

In all most every synchronous transceiver architecture design, a crystal oscillator is pre-requisite, which provides the time definition to the transceiver. On the other hand, the on-chip oscillator can not provide precise and accurate timing information due to the process-voltage-temperature (PVT) variations. The frequency of an on-chip oscillator can vary up to 15%, which can be controlled using off-chip calibration. In contrast, crystal oscillator frequency variation is typically $< 0.005\%$, which accounts for < 50ppm. Crystal oscillators have quality factor (Q) in the range $10^4 - 10^6$. External passive and active temperature compensation and control can lead to temperature coefficient under 1ppm/^{0}C.

These merits of crystal oscillator comes with the additional cost and increased power budget. To upconvert the crystal frequency up to the Nyquist rate and to make it temperature stable, dedicated on-chip circuits are required. Hence, with the asynchronous transceiver design, which is the transceiver without the crystal oscillator, there is the possibility to improve the margin over power consumption, cost and ultimately could lead to complete SoC design.

For the bio-medical application like capsule-endoscopy, a new code-based frequency-detection asynchronous transceiver architecture is modeled and analyzed on Simulink Matlab. The transceiver uses the OOK modulation, and OOK is opted to save the transmission power as, during the low-bit interval of the data, zero power is transmitted. Band of frequencies ranging from 400-500 MHz shows minimum attenuation as projected by the human body model. Hence, a 450 MHz carrier with a 1 Mbps data rate is chosen for transmission. The clock and data recovery circuit used in the model can lock onto the frequency and recover data and clock correctly.

For the actual implementation of the transceiver on-chip, 1.8 GHz oscillator is designed for which new inductors are fabricated, characterized, and their impact on oscillator phase noise is studied. Dividing 1.8 GHz by a factor of four provides the required 450 MHz carrier.

RF front-end of the receiver chain is designed, which has a low noise amplifier (LNA), active balun, and a differential mixer. All these circuits after integration consume more than 20 mW for a 3.1 dB noise figure of the RF front-end. To improve the senstivity and reduce

the power consumption of the front-end, a new single to differential LNA is proposed. For 1.25 dB of noise figure, LNA consumes only 7.9 mW. Later the passive mixer on top of the same LNA is implemented, which reuses the LNA current. With this topology, the complete front-end design gives 2.5 dB of noise figure for the same power consumption.

To further improve the sensitivity of the RF front-end, a new sub-1 dB noise-figure ESD-safe LNA topology is proposed. The proposed LNA is fabricated in 130 nm CMOS process. The LNA is lab-tested for 2.5 kV HBM ESD zap and has passed the JEDEC standards within a 10% margin of its initial diode characteristics. LNA is characterized for a 0.9 dB noise figure at 900 MHZ for 5.2 mW of power consumption. LNA uses a single inductor to achieve input matching and a total of only two passives, thereby saving on the active area requirements.

A hybrid circuit of this very-low noise figure LNA is implemented, which can be switched to the oscillator mode. Therefore, the same circuit is used as an LNA during the reception and as an oscillator during the transmission. This topology is fabricated in the 65 nm CMOS process. The oscillator can directly modulate the data for OOK or FSK transmission and can also drive the 50 Ω antenna. Therefore, the hybrid circuit can work as a complete transceiver because the LNA and the buffer (used as a mixer) can demodulate the carrier during the receiving mode. During the transmission mode, it can be switched to the oscillator mode, and the oscillator is capable of modulating data and driving the antenna. Hence, omitting the need for SPDT-switches as the same circuit can do transmission and reception both in half-duplex mode.