Title of the Thesis

Design and Analysis of 4H-SiC based Planar Junctionless FETs for sub-10 nm regime.

Abstract

The continuous scaling of conventional MOSFETs has reached its limit because of increased short-channel effects (SCE). At ultra-short channel lengths, short-channel effects such as drain induced barrier lowering, threshold voltage roll off, large leakage currents due to its kT/q (where k is the Boltzmann's constant, T is the temperature and q is the electron charge), subthreshold limit, and the need for abrupt doping profiles become a major bottleneck for battery operated devices. If these SCE's are not mitigated properly, they will result in poor switching behaviour of the CMOS transistors. The multiple-gate MOSFETs have provided an alternative to conventional MOSFETs with their enhanced gate control over the channel, thus improving the SCE and the leakage behaviour. However, fabricating abrupt junctions still remains a major concern as it requires high thermal budgets. The introduction of the junctionless FETs (JLFETs) provides a promising solution to this problem.

The JLFETs do not require abrupt junction profiles unlike the conventional MOSFET. In a JLFET, the doping of source, channel, and drain is identical and is of the order of 1×10^{19} cm^{-3} (for obtaining low source/drain series resistance to realize Ohmic contacts at the source and drain contacts). The JLFETs offer several advantages over conventional MOSFETs, like enhanced immunity over detrimental short channel effects, better scalability, simple fabrication process with reduced thermal budgets and excellent OFF-state characteristics due to volume depletion. The JLFET behaves as a gated resistor, controlled by the applied gate to source voltage. At lower gate voltages, the channel region in a JLFET is fully depleted due to the work function difference between the gate and the channel, as a result the device remains in OFF-state. When the gate voltage is greater than the threshold voltage, the thickness of the depletion region in the channel decreases allowing the current to flow from the drain to the source.

Since, the channel doping is too high, it becomes difficult to achieve volume depletion with gate electrodes of practically realizable work functions (3.9 eV - 5.5 eV). Realizing volume depletion also puts a stringent constraint on the allowed channel thickness for JLFETs. For the efficient depletion of the semiconductor film in the OFF-state, the semiconductor film has to be ultra-thin so that the gate electric field can penetrate and deplete the entire film. Hence, a suitable combination of doping, thickness, and work function of the gate electrode is required while

designing JLFETs. Therefore, to achieve efficient volume depletion in JLFETs, various techniques such as high- k dielectric as buried oxide, multi-gate and gate-all-around (GAA) architectures have been experimentally studied. These techniques helped to improve the electrostatic control of gate over channel. However, the volume depletion of the channel region results in considerable overlap of the conduction band of the drain region with the valence band of the channel region. This band overlap triggers the lateral band-to-band tunneling (L-BTBT) of electrons from the channel region to the drain region in OFF-state ($V_{GS} < V_{Th}$), which is the dominant mechanism for gate induced drain leakage (GIDL) in JLFETs.

The L-BTBT actuates a parasitic bipolar junction transistor (BJT) action in the lateral direction with the hole-rich channel region acting as the P-type base, the N^+ source extension region acting as the emitter and the N^+ drain extension region acting as the collector region. The L-BTBT is quite detrimental to the scaling of the JLFETs and is more pronounced in the efficient gate control architectures. As a result, the NW and NT JLFET architectures suffer from an enhanced parasitic BJT action. The NT JLFET exhibits a larger OFF-state current compared to NW JLFET owing to the presence of the core gate which enhances the LBTBT. The tunnelling current acts as the base current and is amplified by the gain of the parasitic BJT. Thus, the L-BTBT induced BJT action considerably increases the OFF-state current of the NW as well as NT JLFET architectures and hinders their scaling and usage for low power applications. As a result, the JLFETs suffer from a severe degradation in the I_{ON}/I_{OFF} ratio and the proficient gate control in NW and NT architectures is, therefore, not favourable from the perspective of L-BTBT induced GIDL. Thus, L-BTBT needs to be alleviated for the adoption of the emerging FET topologies. Researches have proposed architectures like bulk planar JLFETs, hybrid channel JLFETs and SOI-substrate to mitigate the L-BTBT impact. However, the gain diminishes as the drain-to-source voltage (V_{DS}) is increased. Also, the architectures do not work for channel lengths in sub-10 nm regime. Hence, it becomes even more important and relevant to mitigate the L-BTBT issue for future CMOS scaling.

Therefore, in this doctoral work, various solutions are proposed to mitigate the L-BTBT induced parasitic BJT action and avoid use of complex and costly fabrication architectures like nanowire, gate-all-around and nanotube for sub-10 nm regime. We propose use of P^+ pockets near the source-channel and drain-channel interfaces to realize a planar 4H-SiC JLFETs for sub-10 nm regime. We also show using calibrated device simulations that the 4H-SiC JLFETs exhibit reduced impact of Interface traps unlike conventional 4H-SiC MOSFETs. The proposed 4H-SiC planar JLFETs also exhibit better high-voltage break-down characteristics as compared to conventional Si JLFETs. Moreover, recent studies have shown channel mobility in conventional MOSFETs as

high as ~100 cm^2/Vs, which makes 4H-SiC JLFETs very attractive as a future device for low-power and low-leakage applications, specially the IoT and automotive applications.

We also did a comprehensive analysis of various leakage mechanisms governing the subthreshold performance of sub-10 nm regime 4H-SiC planar JLFETs taking into account (a) Gate induced drain leakage (GIDL) mechanism (b) direct gate tunneling, and (c) inefficient volume depletion. Unlike the silicon-based JLFETs which are significantly impacted by the L-BTBT induced GIDL, the 4H-SiC JLFETs are quite immune to the L-BTBT induced GIDL due to their wider bandgap compared to the silicon. Hence, the leakage mechanism in 4H-SiC can essentially be dictated either by the gate leakage due to the direct tunneling through the thin gate dielectric or the inefficient volume depletion especially for the sub-10 nm regime. Therefore, we have presented the design guidelines for sub-10 nm regime, which can be used for designing required channel length, channel thickness, and gate oxide thickness to have the effective volume depletion.

We have also developed a drain current model for Dual-Material gate JLFET under full and partial depletion conditions using Finite-Differentiation method. We used Finite-Differentiation method to reduce the complex 2-D poison's equation to simple 1-D poison's equation, which could potentially help in reducing the significant computational efforts.