Department of Electrical Engineering
Indian Institute of Technology, Delhi
Hauz Khas, New Delhi 110016

NIQ no. IITD/EE/RP03438G/1 Due Date: **15.4.2019, 5 PM**

Notice inviting quotations for fabrication of a custom integrated circuit on a 65 nm CMOS process

Quotations are invited for fabrication of a custom integrated circuit on a 65 nm CMOS process. The required specifications are given below.

Required Specifications for fabrication of a custom integrated circuit on a 65 nm CMOS process

1. A custom design should be fabricated on a UMC 65 nm CMOS process.
2. The total area of the integrated circuit is 1875 μm $\times$1875 μm, including the die-seal ring.
3. A total of at least 20 parts are required. The parts should be diced from the wafer.
4. No packaging is required.

Dr. S. Chatterjee
(Chairperson, purchase committee)

Terms and Conditions

1. The quote should reach the following address on or before **15.4.2019, 5 PM**. Quotations can be submitted physically in a sealed envelope, or electronically, through email to `shouri@ee.iitd.ac.in`. Internet-based online quotations are also permissible.

   Dr. S. Chatterjee
   VLSI Design Tools and Technology
   Block IV, Room 202
   IIT Delhi, Hauz Khas
   New Delhi, 110016

2. Please quote prices for FOB New Delhi.

3. Quote should be in Indian Rupees for Indian agents, or in foreign currency, for foreign agents, and needs to be valid for at least three months.

4. Please specify all of your terms and conditions clearly, including delivery period.

5. Mode of payment for purchases in foreign currency are through irrevocable letter of credit, or through wire transfer on receipt of goods. Only bank charges within India are payable by IIT Delhi, all bank charges outside India are the responsibility of the seller. For purchases in INR, payment is only on delivery.

6. Please mention your terms and conditions.

Dr. S. Chatterjee
(Chairperson, purchase committee)