DEPARTMENT OF COMPUTER SCIENCE AND ENGINEERING

NIQ No. CSE/RP02177/5 **Due Date: 28th Feb 2012**

We are interested in procuring **2 Nos.** of Cognitive - Low Band Systems. The specifications for these are listed below:

Specifications for a single High Performance Cognitive Low Band System (need to multiply by 2 Nos)

Each system must consist of (a) a Digital Processing Module, (b) a Data Conversion Module, (c) **TWO** tunable Radio Frequency Low-Band modules (one of which can be in RX operational mode only), (d) Antennas, and (e) 1-year Software Licenses

a) Digital Processing Module

Texas Instruments TMS320DM6446 DM SoC

- 594-MHz C64x+ clock rate
- 297.0-MHz ARM926EJ-S clock rate
- Eight, 32-bit, C64x+ instructions/cycle
- 4,752 C64x+ MIPS
- Fully software-compatible With C64x /ARM9

Xilinx SX35 Virtex-4 FPGA or better

- Maximum of 34,560 logic cells
- Maximum of 192 XtremDSP slices

Interfaces

- RJ45 10/100-Mbps Ethernet
- JTAG interfaces for DSP and FPGA
- Stereo audio codec (8 kHz to 48 kHz)
- RS-232 interface
- Human-machine interfaces (LEDs, buttons, DIP switches)
- SD card interface (driver not developed)
- USB interface (driver not developed)

Memory • 128 MB NAND flash memory

- 128 MB DDR2 SDRAM

b) Data Conversion Module

- Analog-to-digital converters • ADS5500 from Texas Instruments (×2)
- • Guaranteed maximum sampling rate of up to 125 MSPS (14-bit resolution)
- Analog inputs 50-Ω SMA connectors
- Optional analog inputs
- • AC coupled
- • 1-MHz to 150-MHz analog input bandwidth (–3 dB)
- • –24.2-dBm to 6.4-dBm full-scale input (depending on the programmable gain/attenuator settings)
- • 88-dBc SFDR at 70 MHz Fin(for a bandwidth of 30 MHz and a gain of 8.5 dB)
- • 77-dBc SFDR at 70 MHz Fin (for a bandwidth of 30 MHz and a gain of 31 dB)
- • Interchannel crosstalk insulation of 92 dBc at 70 MHz Fin (with a gain of 10

dB)

- • Interchannel crosstalk insulation of 72 dBc at 70 MHz Fin (with a gain of 31 dB)
- DC coupled
- • DC to 65-MHz analog input bandwidth (–3 dB)
- • 10.6-dBm full-scale input (no programmable gain/attenuator available)
- • 105-dBc SFDR at 1 MHz Fin (for a bandwidth of 2 MHz)
- • 72.04-dBc SFDR at 30 MHz Fin
- • 88-dBc SFDR at 30 MHz Fin (for a bandwidth of 10 MHz)
- • Interchannel crosstalk insulation of 98 dBc at 30 MHz Fin
- Dual-channel digital-to-analog converters
- • Dual-channel DAC5687 from Texas Instruments (×1)
- • Guaranteed maximum interpolating sampling rate of up to 500 MSPS (16-bit resolution)
- • 1×, 2×, 4×, or 8× interpolating factors
- • Integrated NCO, mixer, and digital filters
- • Integrated independent programmable amplifiers per channel
- • Integrated quadrature mode or independent dual channel
- Analog outputs 50-Ω MMCX connectors
- Optional analog outputs
- AC coupled
- • 0.3 MHz to 240 MHz analog output bandwidth (–3 dB)z
- • –21.4-dBm to 2.72-dBm full-scale output (minimum to maximum programmable gain)
- • 76.91 dBc SFDR at an IF of 30 MHz (for a bandwidth of 60 MHz, at full scale, interpolationX4, fine mixer, and an
- Fs of 500 MHz)
- • 77.21 dBc SFDR at an IF of 70 MHz (for a bandwidth of 40 MHz, at full scale, interpolationX4, fine mixer, and an
- Fs of 500 MHz)
- • Interchannel crosstalk insulation of –75 dBc at 30 MHz/70 MHz IFout
- • SNR of 65 dB at 30 MHz IFout, 59.2 dB at 70 MHz IFout
- DC coupled
- • DC to 240 MHz analog output bandwidth (–3 dB)
- • –23-dBm to 0-dBm full-scale output (minimum to maximum programmable gain)
- • 75 dBc SFDR at an IF of 30 MHz (for a bandwidth of 60 MHz, at full scale, interpolationX4, fine mixer, and an Fs
- of 500 MHz)
- • 70 dBc SFDR at an IF of 70 MHz (for a bandwidth of 40 MHz, at full scale, interpolationX4, fine mixer, and an Fs
- of 500 MHz)
- • Interchannel crosstalk insulation of –53.2 dBc at 30 MHz/70 MHz IFout
- • SNR of 54 dB at 30 MHz IFout, 49 dB at 70 MHz IFout
- Sampling clocks, synchronization, and trigger options
- • Software-selectable onboard or external reference clock

- • Software-selectable PLL or external ADC/DAC clock
- • Maximum 225 Fs rms output jitter onboard PLL
- • 1 GHz to 1.5 GHz onboard VCO to generate virtually any frequency
- • Phase noise of 110 dBc at 10 kHz for a 125-MHz generated clock output
- Xilinx LX25 or SX35 Virtex-4 FPGA • Maximum of 34,560 logic cells
- • Maximum of 192 XtremeDSP slices
- Offboard communication channels 32-bit, user-defined external Virtex-4 single-ended GPIO-32 header

c) Tunable Radio Frequency Module Low-Band (X2):

NOTE: EACH UNIT SHOULD SHIP IN WITH 2 RF MODULES.

General

- Supply voltage: 12 V
- Supply current: 0.6 A
- Power consumption: 7.2 W
- Up to 80 dB of isolation between TX and RX
- 3-dBm maximum transmit power at P–1 dB
- GPIO-16 control interface (SPI ports, others)
- Supports configuration from the SFF SDR evaluation module's GPIO-16 port
- Full-duplex transceivers (separate RX and TX antennas)
- Software-selectable reception bandwidths: 5 MHz or 20 MHz

Low-band channel

- RX/TX IF center frequency: 30 MHz
- Reference clock input: 4 MHz to 100 MHz, –20 dBm to 10 dBm
- Reference clock output: 10 MHz, 10 dBm

RF frequency range

- TX: 0.2 GHz to 1.0 GHz
- RX: 0.2 GHz to 1.0 GHz

RF input

- Gain: 50 dB (RX selectable filter: 20 MHz)
- Gain: 46 dB (RX selectable filter: 5 MHz)
- Noise figure : 5 dB
- Phase noise at 10 kHz from carrier: –75 dBc/Hz (RF: 425 MHz)
- Phase noise at 100 kHz from carrier: –103 dBc/Hz (RF: 425 MHz)
- Minimum detectable signal: –102 dBm (bandwidth: 5 MHz)

RF output

- Carrier suppression: –55 dBc
- Sideband suppression: –37 dBc
- Phase noise at 10 kHz from carrier: –83 dBc/Hz (RF: 425 MHz)
- Phase noise at 100 kHz from carrier: –109 dBc/Hz (RF: 425 MHz)
- Gain: 8 dB
- IP3 output: 25 dBm

d)Antennas

Supporting 0.2 to 1 GHz

Warranty: 12-month software updates and technical support [Response time 1-3

business days]), 12-month hardware warranty

e) **Software**

- Board Software Development Kit with full license
- Model based development kit with full license
- FPGA target MBDK license

Terms and Conditions

(i) Bids should be properly sealed. Technical and Commercial bids must be sealed in separate sealed envelops packed in one big sealed envelop.

(ii) For Foreign Currency bids, Bids must be made on FOB basis.

(iii) Complete bill of material to be attached with Technical Bid.

(iv) Technical Compliance chart should be strictly attached with Bid.

(v) Validity of quotation should be minimum 90 days from the date of bidding.

(vi) Authorisation from the OEM in case of bids by Authorised resellers must be attached.

(vii) Sealed quotations with technical and financial bids in separate envelops must reach the office of HOD, Deptt. of CSE, IIT Delhi positively by 28th Feb, 2012 by 5.00 PM

(viii) Warranty should be mentioned clearly.

(ix) Payment terms should be clearly mentioned in the bid.

(x) Quotations not sent in separate covers for technical and commercial bids are bound to be rejected.

(xi) IIT Delhi Reserves the right to accept or reject any quotations without assigning any reasons thereof.