DEPARTMENT OF ELECTRICAL ENGINEERING

INDIAN INSTITUTE OF TECHNOLOGY DELHI

Ref. No. ***No. IITD/EE/OCL/2012*** Date: 05.03.12

NOTICE INVITING QUOTATIONS

Sub: Purchase of Dual Channel Pulse/ Pattern Generator 650 MHz

Sealed quotations are invited for Purchase of **Dual Channel Pulse/ Pattern Generator 650 MHz** from the authorized dealers/ suppliers/ manufacturers in the sealed envelopes subscribing our reference No. and due date in the name of undersigned.

Technical Details

No. of channels	Two
Frequency range	170 kHz - 650 MHz
Variable delay range	1.5 ns - 1 ms
Period RMS - jitter	0.00 ns to 3.00 µs
Pulse Width range	750 ps to (period - 750 ps)
Amplitude range	100 mV - 2.5 V
Transition time range	(10/90) 500 ps typ.fixed
Pulse and Data Generator	Integrated
Source impedance	50 Ω
Period range	(f < 170 kHz: 1.5 ns to 1.0 ms)
Width range	1.25 ns to 3 micro s
Width resolution	4 digits (2 ps best case)(f < 170 kHz: 0.05% of period)
Duty Cycle	0.1%-99.9%
Width accuracy	+_ (100 ppm + 200 ps)
	(f < 170 kHz: 0.06% of period)
Width jitter	0.001% + 15 ps
Add, variable delay range	0 to 3.00 µs independent of period
	(> 3 µs: one to 1 period)
Delay resolution	4 digits (2 ps best case)
	(f < 170 kHz: +_ 0.05% of period)
Delay accuracy	+_ (0.01% + 100 ps) relative to zero delay
	(f < 170 kHz: +_ 0.035% of period)
Delay jitter	0.001% + 15 ps
Fixed delay:	
• Clk in to out	53 ns
• Ext. in to out	54 ns + 0 to 1 period 1
Transition time range (10/90)	Fixed
Minimum transition (10/90)	500 ps
At ELC levels	< 500 ps (400 ps typ.)
Deskew range	+_ 25 ns
Amplitude Level	0.10 Vpp to 2.50 Vpp
• Window	-2 .00 V to +3.00 V
• Accuracy	+_ (5% +150 mV)
• Resolution	3 digits (10 mV best case)
Output impedance.	50 Ω +_ 5% typ.
Max. external voltage	-2.0 to +4.0 V
Short circuit current	-80 mA to +120 mA

Baseline noise	8 mV RMS typ.
Overshoot/preshoot/ringing	+_ (5% + 100 mV) of amplitude typ.
Connectors	SMA (f) 3.5 mm.
Data Formats	RZ,NRZ,DNRZ
Termination voltage	-2.10 V to 3.30 V.
Input sensitivity	< 400 mV typ.
Max. input voltage	-3 V to + 6 V.
Input transitions	< 20 ns. Only valid for clock input/PLL reference.
Reference	The internal PLL is locked to the 1, 2, 5 or 10 MHz.
External clock	The output period is determined by the signal at clock input.
Trigger output	At start of every pattern
Trigger Levels	1Volt-GND, ECL,PECL,Selectable
Trigger Transition Time	1ns or less
Pattern	PRBS upto 2^15-1 and memory patterns.
Pattern Generator Software	Software for generating and loading patterns
Cables SMA(m) to SMA (m)	4 Nos.
2.4 mm female to APC-3.5 female adapter	One No.

Terms and conditions:

1. Please submit TECHNICAL and FINANCIAL bids in separate sealed envelopes. Mark the two envelops clearly as "Technical Bid" and "Financial Bid". Both the sealed envelops should be sent in a single sealed envelope clearly marked as **'Quotation for Dual Channel Pulse/ Pattern Generator'**

2. The Quote should reach the following address on or before 19-03-12 Up to 10 AM

   Prof. Vinod Chandra
   Optical Communication Lab
   Block II, Room No. 203
   Department of Electrical Engineering
   IIT Delhi
   Hauz Khas New Delhi 110016

3. Quote should be valid for at least three months.

4. Price quoted should be FOB inclusive of all taxes and duties in both USD and INR.

5. VAT and TIN No. of the supplier should be clearly mentioned.

6. If the quote is being submitted by the representative of the principals or manufactures themselves, please attach a valid agency certificate/dealership certificate authorizing the agent to quote on behalf of the manufacturer or principles. Proprietary item certificate from manufacturer may be submitted if applicable.

7. Produce compliance certificate for technical specifications.

8. The companies who comply with technical specifications in technical bid will be invited for Demonstration of technical features to the committee at its own expenses before issuing of supply order at date and time to be specified.

9. The Financial bid of only those companies who comply with the Technical Specification in Technical bid and satisfactory demonstration of technical features to the committee will be considered.

10. Commercial bid must include clearly applicable taxes, Delivery Schedule, Quotation validity, warranty and payment terms.

11. Bidder/supplier would be fully responsible for installation of the above equipment. Appropriate wires, industrial plugs, tops etc. needed for installation would be provided by the supplier

12. The bidder must be a manufacturer or authorized service provider capable of providing technical Service and repair of the product.

13. The product must be ISO certified.

14. The Institute reserves the right to accept or reject any quotation or all quotations without assigning any reasons thereof.

Prof. Vinod Chandra

Prof. EE Deptt