Notice inviting quotations for packaging of custom integrated circuit fabricated in a 0.18 $\mu$m CMOS process

Sealed/online/e-mail quotations are invited for packaging of custom integrated circuit fabricated in a 0.18 $\mu$m CMOS process. The required specifications are given below.

**Required Specifications for packaging of custom integrated circuit fabricated in a 0.18$\mu$m CMOS process**

The custom designed microchips in AMS 350nm needs to be wire bonded to packages. The specification of the packages are as follows:

1. Package: Open cavity Pin Grid Array (PGA) Ceramic
2. No. Of pins: 84
3. Package size (one side): 1.320 inches
4. Spacing between two corner pins (bottom view): 1.210 inches
5. LID size (internal): 0.680 inches
6. LID size (external): 0.740 inches
7. Pin size: 0.050 inches
8. Pin length: 0.190 inches
9. Spacing between two pins: 0.100 inches

Dr. M. Sarkar  
(Chairman, purchase committee)
Terms and Conditions

1. The quote should reach the following address on or before 11.01.2017, 5 PM.
   Dr. M. Sarkar  
   Electrical Engineering Department  
   Block II, Room 333  
   IIT Delhi, Hauz Khas  
   New Delhi, 110016  

2. Please quote prices for FOB New Delhi, inclusive of all taxes and duties.  

3. Quote should be in Indian Rupees for agents of Indian manufacturers, or in foreign currency, for agents of foreign manufacturers, and needs to be valid for at least three months.  

4. Please specify all of your terms and conditions clearly, including delivery period.  

5. Mode of payment for purchases in foreign currency are through irrevocable letter of credit, or through wire transfer on delivery. Only bank charges within India are payable by IIT Delhi, all bank charges outside India are the responsibility of the seller. For purchases in INR, payment is on delivery.  

6. The Institute reserves the right to accept or reject any or all quotations without assigning any reasons thereof.

Dr. M. Sarkar  
(Chairman, purchase committee)